Claims

What is claimed is:

1. A method used to form a semiconductor device, comprising:

forming a container capacitor bottom plate layer which defines a receptacle and a rim, said rim defining an opening to an interior of said receptacle, with said rim and said receptacle having a first texture;

forming an inhibitor layer over said rim of said container capacitor bottom plate layer while a majority of said receptacle defined by said bottom plate layer remains free from said inhibitor layer; and

with said inhibitor layer over said rim of said bottom plate layer, converting at least a portion of said receptacle defined by said bottom plate layer to have a second texture which is rougher than said first texture, while maintaining said first texture of said first region with said inhibitor layer.

2. The method of claim 1 further comprising removing said inhibitor layer subsequent to said conversion.

3. The method of claim 1 further comprising:

forming a cell dielectric layer over said inhibitor layer; and

forming a capacitor top plate layer over said cell dielectric layer and over said inhibitor layer.

4. The method of claim 1 further comprising forming said container capacitor bottom plate layer such that said rim and said receptacle are generally continuous, each with the other.

5. The method of claim 1 further comprising:

forming said inhibitor layer at a bottom of said interior of said receptacle during said formation of said inhibitor layer; and

maintaining said first texture of said bottom of said interior of said receptacle subsequent to conversion of said portion of said receptacle to have said second texture.

6. A method used to form a semiconductor device comprising:

providing a container capacitor bottom plate having, in cross section, two substantially vertically-oriented sides and a bottom, and further having a recess defined by said substantially vertically-oriented sides and said bottom and an opening to said recess defined by an upper region of said cross sectional vertically-oriented sides;

forming a dielectric layer over said upper region of said vertically-oriented sides; and

subsequent to forming said dielectric layer, converting at least a portion of said bottom plate to hemispherical silicon grain (HSG) polysilicon while said upper region of said vertically-oriented sides covered by said dielectric layer remains free from said HSG polysilicon conversion.

7. The method of claim 6 further comprising removing said dielectric layer from said upper region of said vertically-oriented sides subsequent to converting said portion of said bottom plate to HSG polysilicon.

8. The method of claim 6 further comprising forming said dielectric layer on said upper region of said vertically-oriented sides from low silane flow oxide.

9. The method of clam 6 further comprising forming said dielectric layer on said upper region of said vertically-oriented sides from a material selected from the group consisting of borophosphosilicate glass, tetraethyl orthosilicate, and phosphosilicate glass.

10. The method of claim 6 further comprising:

subsequent to converting at least said portion of said bottom plate to HSG polysilicon, forming a capacitor cell dielectric conformal with said vertically-oriented sides and with said dielectric layer; and

subsequent forming said capacitor cell dielectric, forming a polysilicon capacitor top plate conformal with said capacitor cell dielectric, said vertically-oriented sides, and with said dielectric layer.

11. A method used during the formation of a semiconductor device comprising:

providing a patterned deposited oxide layer over a semiconductor substrate assembly, said deposited oxide layer comprising a recess therein;

forming a blanket smooth polysilicon layer conformal with said patterned deposited oxide layer;

forming a blanket protective layer within said recess and over said blanket smooth polysilicon layer;

planarizing said protective layer and said smooth polysilicon layer to remove said smooth polysilicon layer from an upper surface of said deposited oxide layer;

anisotropically etching said deposited oxide layer to form a horizontally-oriented surface of said deposited oxide layer at a level below an upper surface of said smooth polysilicon layer, and to form and a vertically-oriented surface of said deposited oxide which covers a vertically-oriented surface of said smooth polysilicon layer;

removing said protective layer from within said recess to expose said smooth polysilicon within said recess;

forming an inhibitor layer over an upper surface of said smooth polysilicon layer to cover said upper surface of said smooth polysilicon layer; and

converting said exposed smooth polysilicon within said recess to roughened polysilicon, while said smooth polysilicon covered by said vertically-oriented surface of said deposited oxide and said upper surface of said smooth polysilicon layer covered by said inhibitor layer remains unconverted.

12. The method of claim 11 further comprising removing said inhibitor layer subsequent to converting said smooth polysilicon to roughened polysilicon.

13. The method of claim 11 further comprising forming a capacitor cell nitride layer and a capacitor top plate layer over said roughened polysilicon layer and said inhibitor layer subsequent to converting said smooth polysilicon to roughened polysilicon.

14. A method used during the formation of a semiconductor device comprising:

providing a patterned deposited oxide layer over a semiconductor substrate assembly, said deposited oxide layer comprising first and second spaced recesses therein;

forming a blanket smooth polysilicon layer conformal with said patterned deposited oxide layer;

forming a blanket protective layer within said first and second recesses and over said blanket smooth polysilicon layer;

planarizing said protective layer and said smooth polysilicon layer to remove said smooth polysilicon layer from an upper surface of said deposited oxide layer and to electrically isolate said polysilicon in said first recess from said polysilicon in said second recess to form first and second container capacitor bottom plates, wherein subsequent to said planarization said upper surface of said deposited oxide is generally planar with an upper surface of said first and second capacitor bottom plates;

removing said protective layer from within said first and second recesses to expose said smooth polysilicon within said recesses;

forming an inhibitor layer over said upper surface of said first and second capacitor bottom plates and over said upper surface of said deposited oxide layer; and

converting said exposed smooth polysilicon within said recesses to roughened polysilicon, while said upper surface of said smooth polysilicon layer covered by said inhibitor layer remains unconverted.

15. The method of claim 14 further comprising removing said inhibitor layer subsequent to converting said smooth polysilicon to roughened polysilicon.

16. The method of claim 14 further comprising forming a capacitor cell nitride layer and a capacitor top plate layer over said roughened polysilicon layer and said inhibitor layer subsequent to converting said smooth polysilicon to roughened polysilicon.

17. A semiconductor device comprising:

a patterned deposited dielectric layer comprising a plurality of recesses therein;

a capacitor bottom plate formed within said recess;

an inhibitor layer covering only an upper region of said capacitor bottom plate such that a lower region of said capacitor bottom plate is not covered by said inhibitor layer, wherein said upper region of said capacitor bottom plate is smooth polysilicon and said lower region of said capacitor bottom plate is roughened polysilicon;

a capacitor cell dielectric layer formed over said inhibitor layer and over said bottom plate; and

a capacitor top plate layer formed over said cell dielectric layer, over said inhibitor layer, and over said capacitor bottom plate.

18. The semiconductor device of claim 17, wherein:

said lower region of said capacitor bottom plate is hemispherical silicon grain (HSG) polysilicon;

said upper region of said capacitor bottom plate is smooth polysilicon; and

said inhibitor layer is oxide.

19. The semiconductor device of claim 18 wherein said inhibitor layer is low silane flow oxide.

20. The semiconductor device of claim 18 wherein said inhibitor layer is nitride.

21. A semiconductor device comprising:

a conductive container capacitor bottom plate layer;

a first portion of said bottom plate layer which defines a receptacle, wherein said first portion of said bottom plate layer comprises a first texture;

a second portion of said bottom plate layer which defines a rim to an interior of said receptacle, wherein said second portion of said bottom plate layer comprises a second texture which is smoother than said first texture; and

a cell dielectric layer formed over said bottom plate layer which contacts said first portion and said second portion of said bottom plate layer.

22. The semiconductor device of claim 21 wherein said container capacitor bottom plate layer comprises a single polysilicon layer.

23. The semiconductor device of claim 22, wherein:

said first portion of said container capacitor bottom plate layer is hemispherical silicon grain (HSG) polysilicon; and

said second portion of said container capacitor bottom plate layer is smooth polysilicon.